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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,571	03/25/2004	Masaya Tarui	02887.0266	4847

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EXAMINER	
SURYAWANSHI, SURESH	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 08/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/808,571	TARUI ET AL.	
	Examiner	Art Unit	
	Suresh K. Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-15 and 17* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948).
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/25/04,4/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 are presented for examination.

Drawings

2. The figure 9 is objected to because it does not show that the source voltage is supplied to the processing part as claimed in claim 15 and disclosed in the specification at page 15, lines 8-14. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4 and 9-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohmori (US Patent 6,647,502).

5. As per claim 1, Ohmori discloses a processor comprising:

a clock signal generator generating clock signals [Fig. 1; clock generator];

an operational processing part performing data processing which is divided into a plurality of execution units, in accordance with the clock signals [Fig. 1; col. 4, lines 30-33, 40-44; here the semiconductor circuit is an operational processing part that is divided into module 4 and module 6 processing data from FIFO 3 and FIFO 5 respectively];

a storage storing data used when each execution unit is executed by the operational processing part [Fig. 1; FIFO 3 and FIFO 5 store data used by the module 4 and the module 6 respectively; col. 9, lines 25-48];

a data amount detector detecting amounts of the data stored in the storage per each execution unit [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; FIFO memories outputting a half empty flag or full flag (amounts of data stored) to the clock controller; col. 9, lines 25-48];

a clock frequency determining part determining a new clock frequency of the clock signals by using the amounts of the data, said clock signals being supplied newly to the operational processing part [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; col. 5, lines 20-67; the clock controller determining a new clock frequency based on the amounts of the data; col. 9, lines 25-48].

6. As per claim 13, Ohmori discloses a control device for a processor comprising:

a clock signal generator generating clock signals [Fig. 1; clock generator];

an operational processing part performing data processing which is divided into a plurality of execution units, in accordance with the clock signals [Fig. 1; col. 4, lines 30-33, 40-44; here the semiconductor circuit is an operational processing part that is divided into module 4 and module 6 processing data from FIFO 3 and FIFO 5 respectively];

a storage storing the data used when each execution unit is executed by the operational processing part [Fig. 1; FIFO 3 and FIFO 5 store data used by the module 4 and the module 6 respectively; col. 9, lines 25-48];

a data amount detector detecting amounts of data in the storage [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; FIFO memories outputting a half empty flag or full flag (amounts of data stored) to the clock controller; col. 9, lines 25-48];

a clock frequency determining part determining a new clock frequency of the clock signals by using the amounts of data, said clock signals being supplied newly to the operational processing part [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; col. 5, lines 20-67; the clock controller determining a new clock frequency based on the amounts of the data; col. 9, lines 25-48].

7. As per claim 14, Ohmori discloses a clock frequency determining method determining a clock frequency supplied to a processor, which comprises an operational processing part processing data in accordance with clock signals and a storage storing the data used when each execution unit is executed by the operational processing part [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; col. 5, lines 20-67; col. 9, lines 25-48], comprising:

detecting amounts of data associated with the respective execution units, said data being stored in the storage [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; FIFO memories outputting a half empty flag or full flag (amounts of data stored) to the clock controller; col. 9, lines 25-48];

determining a new clock frequency to be supplied to the operational processing part on the basis of the result of the detection [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; col. 5, lines 20-67; the clock controller determining a new clock frequency based on the amounts of the data; col. 9, lines 25-48];

generating clock signals supplied to the operational processing part in accordance with a new clock frequency [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; col. 5, lines 20-67; the clock controller determining a new clock frequency based on the amounts of the data; col. 9, lines 25-48].

8. As per claim 15, Ohmori discloses a source voltage controlling method, in which the source voltage is supplied to a processor comprising an operational processing part processing data in accordance with clock signals and a storage storing the data used when each execution unit is executed by the operational processing part [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; col. 5, lines 20-67; col. 9, lines 25-48], comprising:

detecting amounts of data associated with the respective execution units, said data being stored in the storage [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; FIFO memories outputting a half empty flag or full flag (amounts of data stored) to the clock controller; col. 9, lines 25-48];

determining a new clock frequency to be supplied to the operational processing part on the basis of the result of the detection [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; col. 5, lines 20-67; the clock controller determining a new clock frequency based on the amounts of the data; col. 9, lines 25-48];

controlling the source voltage to be supplied to the operational processing part, following to the new clock frequency [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; col. 5, lines 20-67; the clock controller also controls the voltage control circuit; col. 9, lines 25-48].

9. As per claim 2, Ohmori discloses that the execution units include a predetermined execution unit, wherein the data amount detector detects per each predetermined execution unit [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; FIFO memories outputting a half empty flag or full flag (amounts of data stored) to the clock controller; col. 9, lines 25-48].

10. As per claim 3, Ohmori discloses an input port receiving the data to be processed by the operational processing part, wherein the data amount detector detects amount of the data received by the input port [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; FIFO memories outputting a half empty flag or full flag (amounts of data stored) to the clock controller; col. 9, lines 25-48].

11. As per claim 4, Ohmori discloses an output port outputting the data obtained by performing the data processing, wherein the data amount detector detects amount of the data output by the output port [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; FIFO memories outputting a half empty flag or full flag (amounts of data stored) to the clock controller; col. 9, lines 25-48].

12. As per claim 9, Ohmori discloses that the storage includes a plurality of storage regions, each of which stores the data for each execution unit, wherein the data amount detector detects the amounts of the data stored in each storage region, wherein the clock frequency detecting part obtains a plurality of clock frequencies on the basis of the amounts of the data associated with each execution unit, and determines the highest clock frequency among said plurality of clock frequencies as the new clock frequency to be supplied newly to the operational processing part [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; col. 9, lines 25-48].

13. As per claim 10, Ohmori discloses an input port receiving a data to be processed by the operational processing part, wherein the clock frequency detecting part determines the new clock frequency on the basis of the amount of the data in the nearest storage region to the input port among said plurality of storage regions [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; col. 9, lines 25-48].

14. As per claim 11, Ohmori discloses an output port outputting a data after being processed by the operational processing part, wherein the clock frequency detecting part determines the new clock frequency on the basis of the amount of the data in the nearest storage region to the output port among said plurality of storage regions [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; col. 9, lines 25-48].

15. As per claim 12, Ohmori discloses that the clock frequency detecting part includes a source voltage controller supplying a source voltage to the operational processing part, in accordance with the new clock frequency [Fig. 1; col. 3, line 58 -- col. 4, line 7; col. 4, line 49 -- col. 5, line 6; col. 9, lines 25-48].

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohmori (US Patent 6,647,502) in view of Sakurai (US Patent 6,335,870).

18. As per claim 5, Ohmori discloses the invention substantially. Ohmori does not disclose about an execution priority storage storing execution order of the execution units. However, Sakurai clearly discloses how a parameter storage unit can be utilized to allow the setting of the order of priority in the execution of the application program and also controlling variable frequency and variable voltage [Fig. 1, 2 and 3; col. 2, lines 30-40; col. 4, lines 6-34; col. 5, lines 18-30]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to a process to control frequency and voltage of a processing system. Moreover, the disclosed invention of Ohmori will clearly be benefited with Sakurai disclosed method of controlling frequency and voltage of a processing system based on a priority of execution. Thus, the combination will produce a better system for processing data more efficiently.

19. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohmori (US Patent 6,647,502) in view of Aisaka et al (US 2003/0184271; herein after Aisaka).

20. As per claims 6-7, Ohmori discloses the invention substantially. Ohmori does not disclose having a table to indicate a relationship between the amount of data and the clock frequency. However, Aisaka discloses a similar system where the voltage and the clock to a data processing circuit is controlled by a control circuit based on information of required process amount [Fig. 1, 4, 7, and 14; paragraphs 0021, 0051 - 0052, 0060 - 0063, 0076 and 0096]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited reference as both are directed to control voltage and clock frequency of a data processing circuit based on an amount of data. A routineer in the art would be able to modify the invention of Ohmori by utilizing a table. Thus, the combination will produce a better system for processing data more efficiently.

Allowable Subject Matter

21. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.